

# CSCI 210: Computer Architecture

## Lecture 18: Clocks and Timing

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Slides from Cynthia Taylor

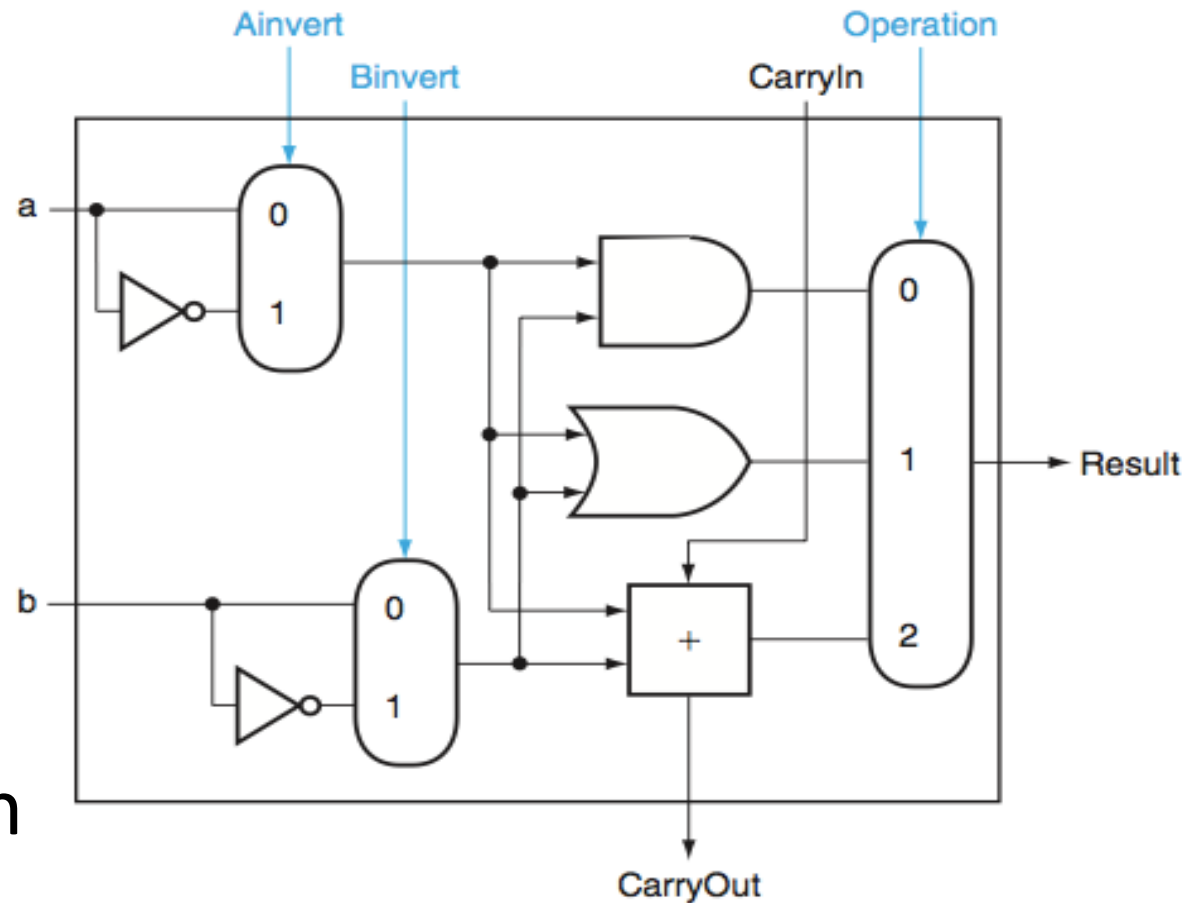
# CS History: Lynn Conway



- Computer Scientist, Electrical Engineer and Transgender Activist born in 1938
- At Xerox Park, worked on *multi-project wafers*, which allowed printing multiple circuit designs on a single silicon wafer
- Co-authored *Introduction to VLSI Systems* in 1981, which became the standard textbook in chip design
- In 1983, developed the *Metal Oxide Semiconductor Implementation Service* system, an internet-based system for rapid-prototyping and small-run fabrication of new chip designs
  - Allowed academics and small businesses to develop their own chips for the first time

# Last Class We Implemented A 1-bit CPU with

- And
- Or
- Nor
- Add
- Subtract
- Set less than
- Overflow detection



# Adding Conditional Branching

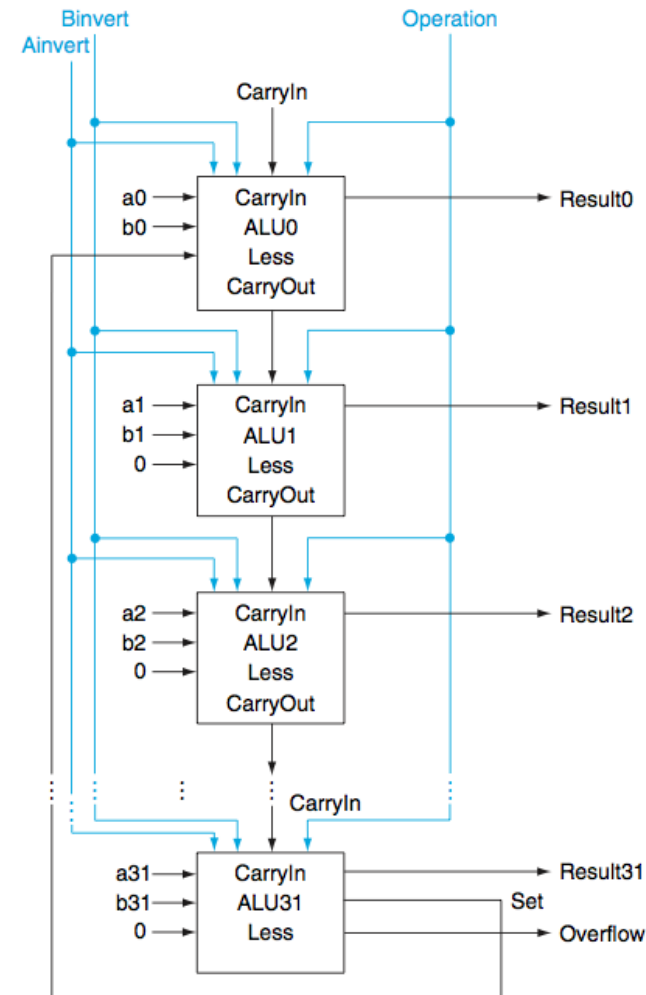
- Want to be able to support beq, bne, etc
- Need to be able to check equality
- If  $a = b$ , then  $a - b = 0$

# Detect 0 in Multi-bit ALU

- Subtract  $a - b$
- Take output from each 1-bit ALU
  - If they are equal, all outputs should be 0

We know Result0-Result31 are all 0 if we perform a \_\_\_\_ operation on Result0 though Result31, and it outputs \_\_\_\_

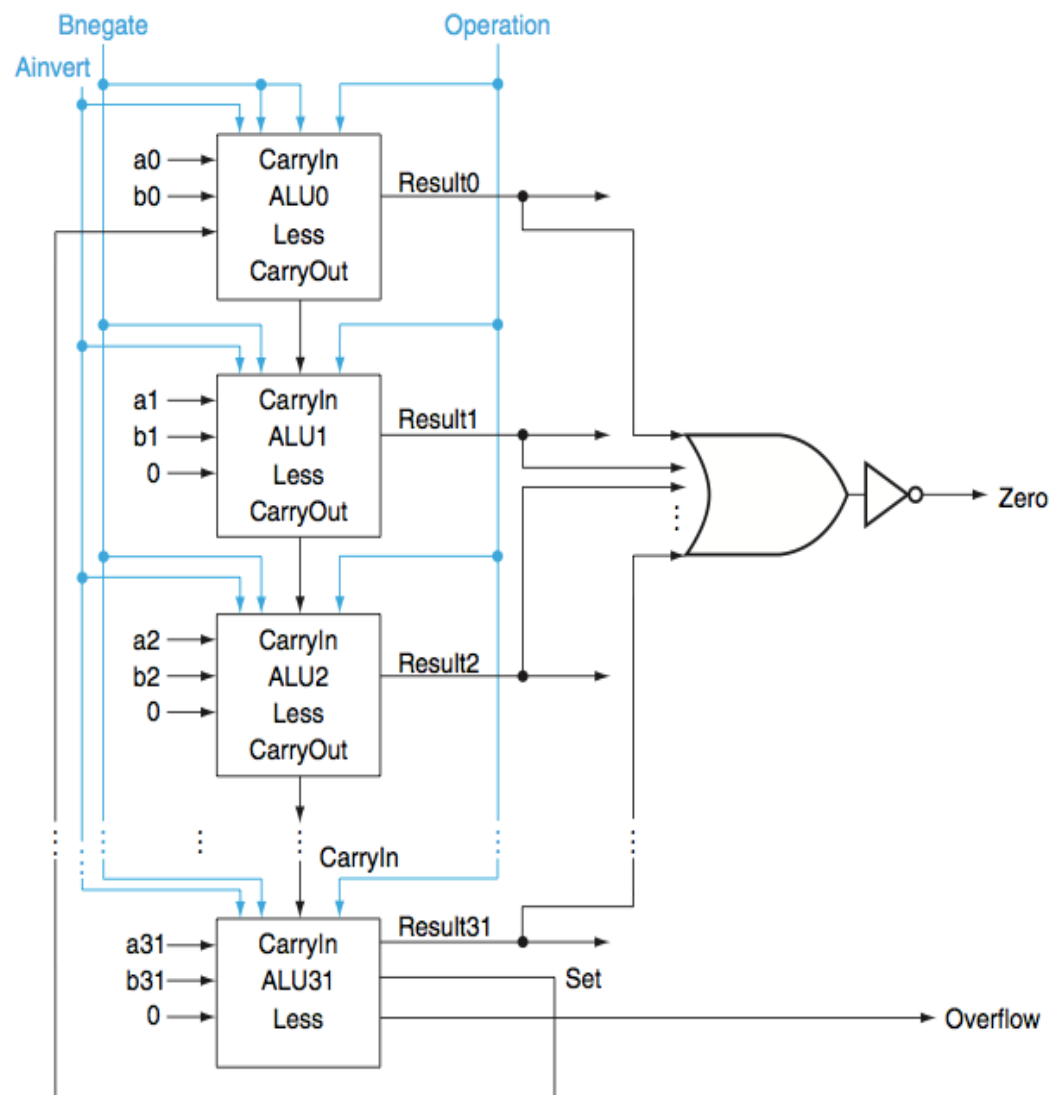
- A. AND, 0
- B. OR, 0
- C. NAND, 1
- D. XOR, 0
- E. None of the above



# Detect 0 in Multi-bit ALU

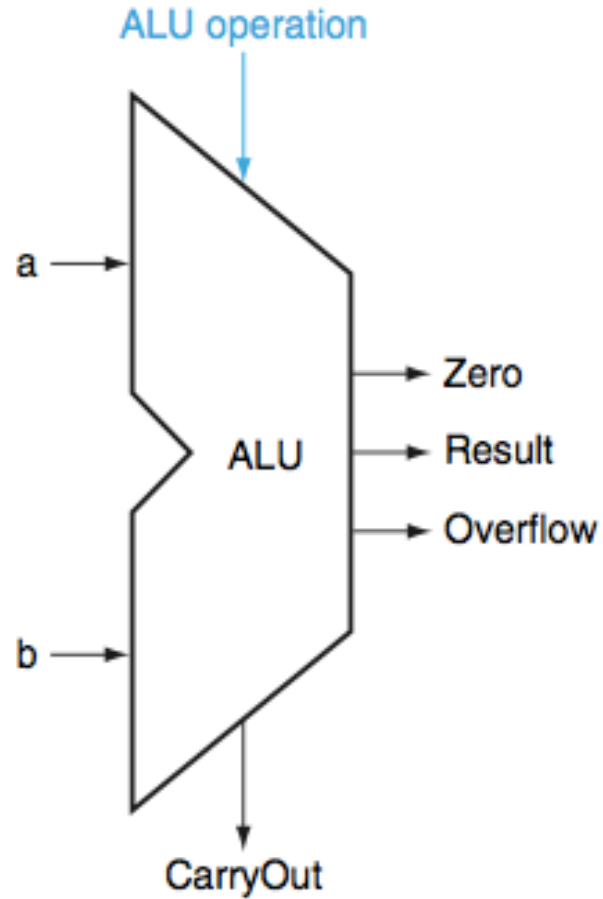
- Subtract  $a - b$
- Take output from each 1-bit ALU
- OR outputs together
  - If any output is 1, result will be 1, else 0
- Negate the result

# 32-bit ALU with zero check



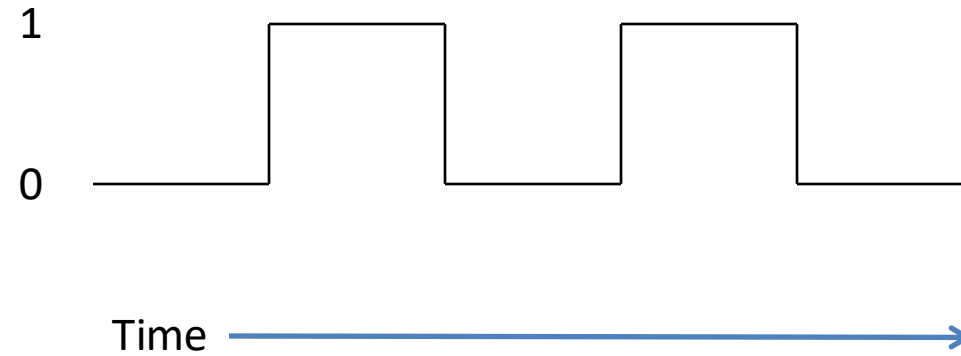


# Symbol for Multi-bit ALU

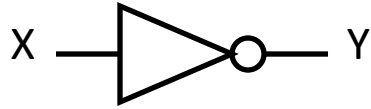


# ALU Questions?

# Logic Gates and Timing Diagrams



Which of the following most closely maps to Y (the output of the inverter)?

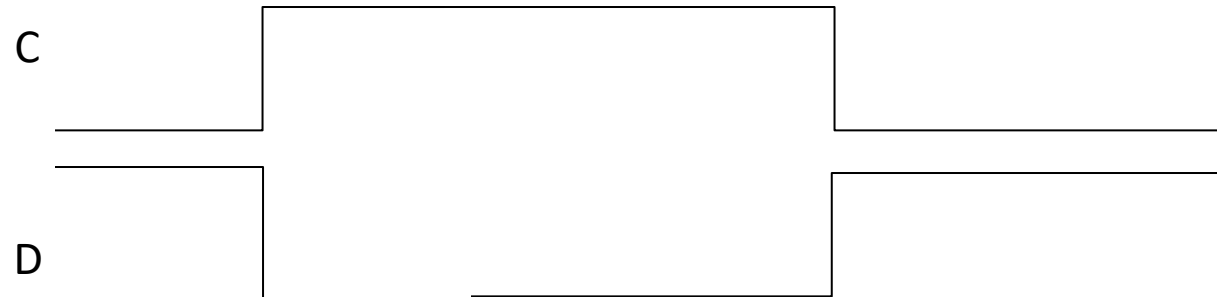
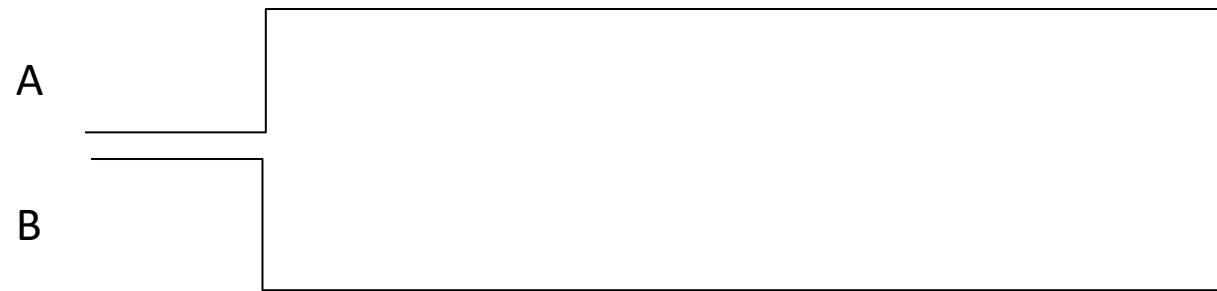


Inverter

X Y

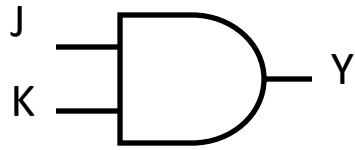
0 1

1 0



E None of the above.

# Select the correct output for Y



AND

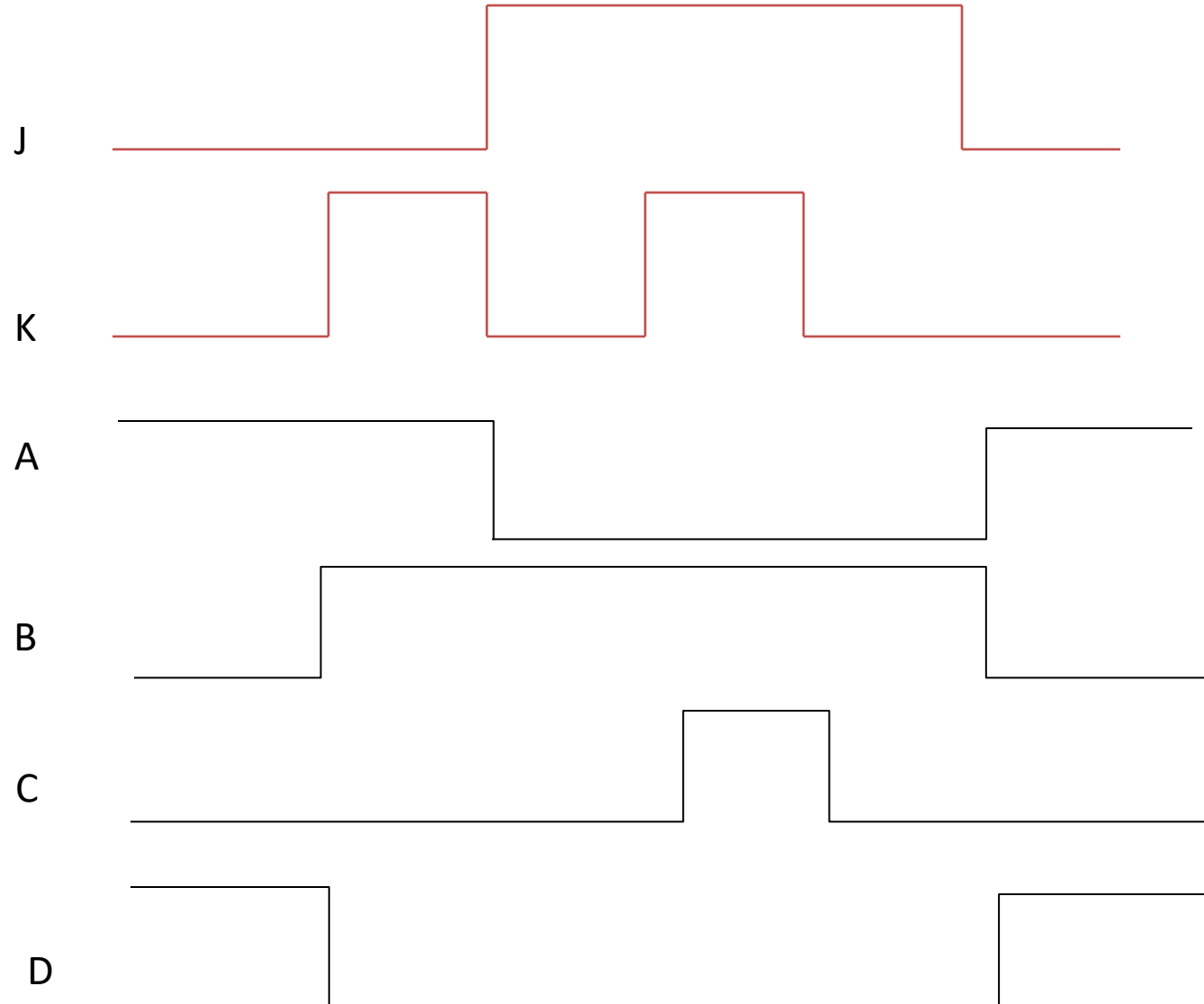
JK Y

00 0

01 0

10 0

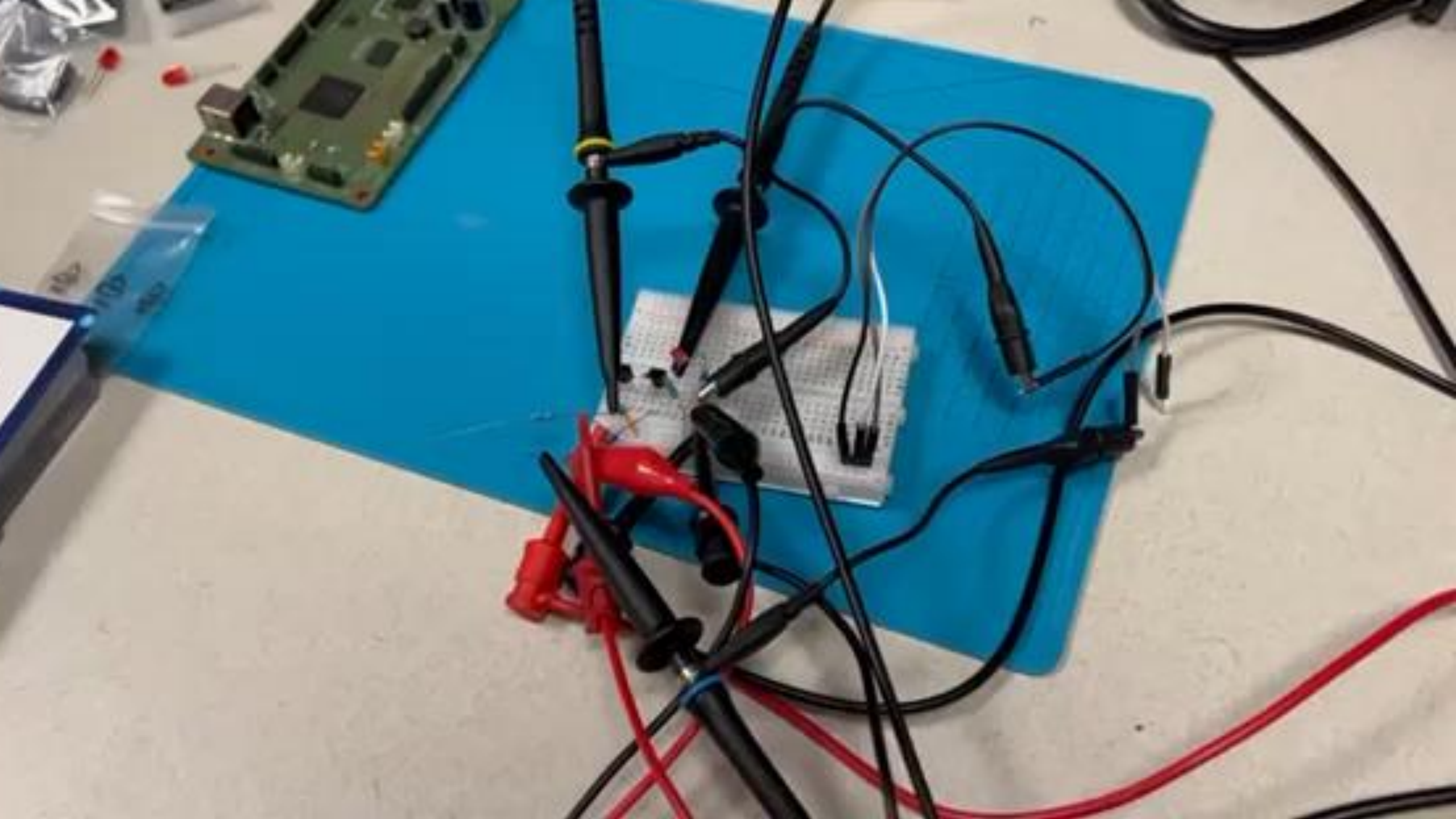
11 1



E None of the above

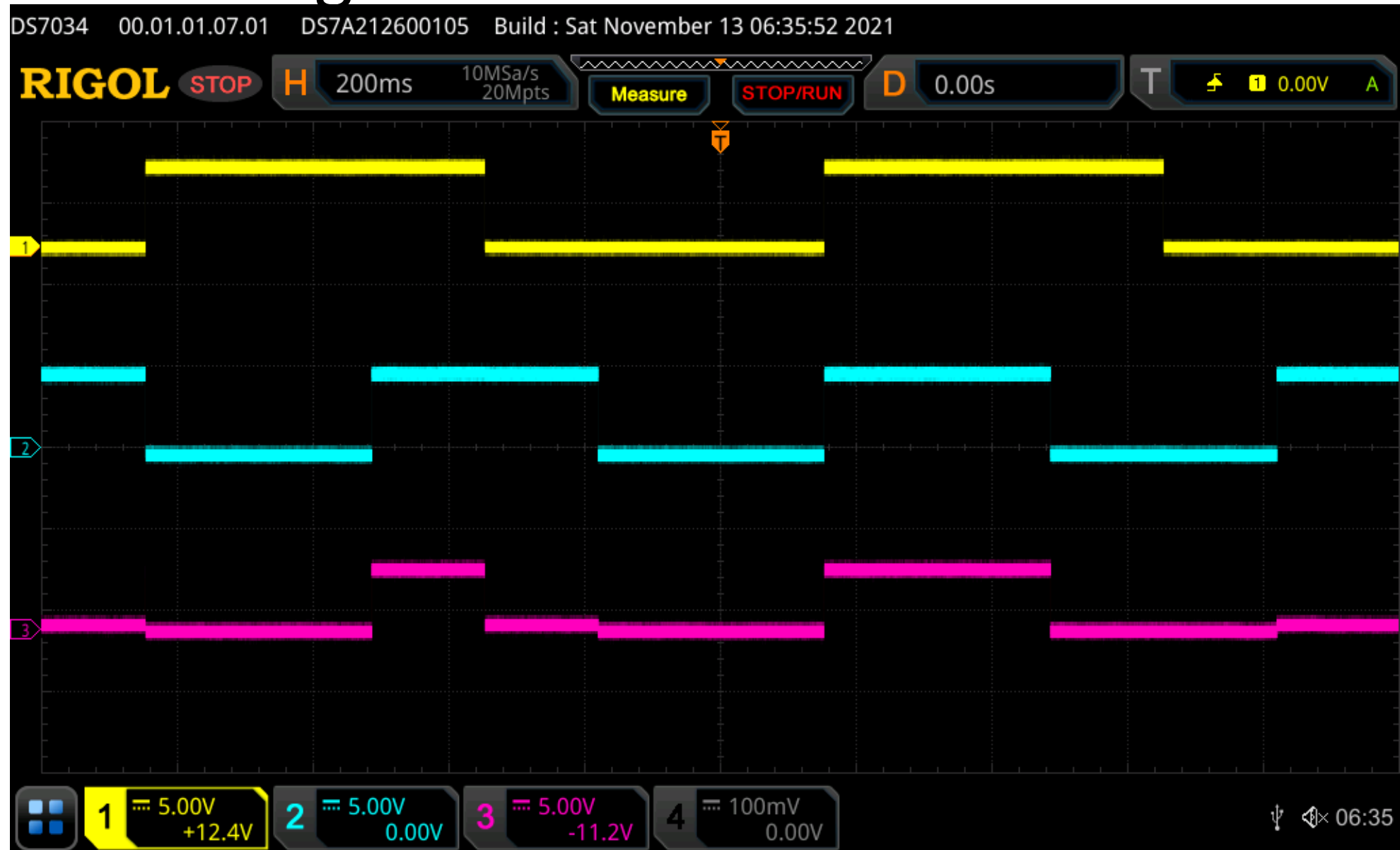
# Timing diagrams and voltage measurements

- Timing diagrams show signals changing over time
- We're looking at logical signals (0s and 1s)
- Voltage levels map to 0s and 1s
- Therefore, we can measure the voltage over time with a tool like an oscilloscope to see this with real hardware



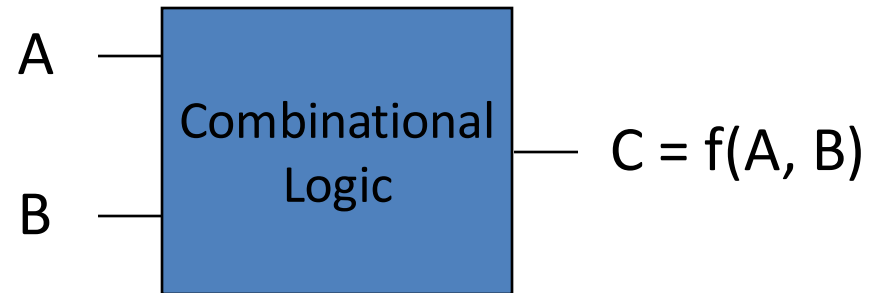
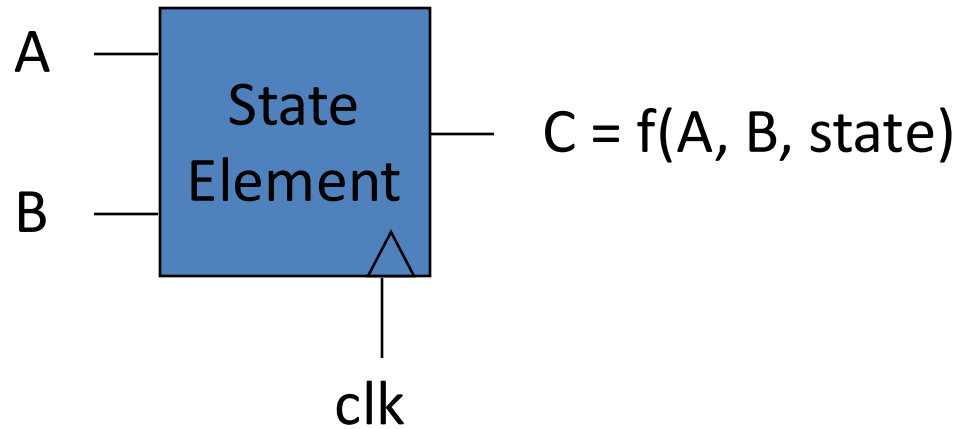
# AND gate waveforms

- Inputs
  - Yellow
  - Blue
- Output
  - Pink





# Two Types of Logic Components



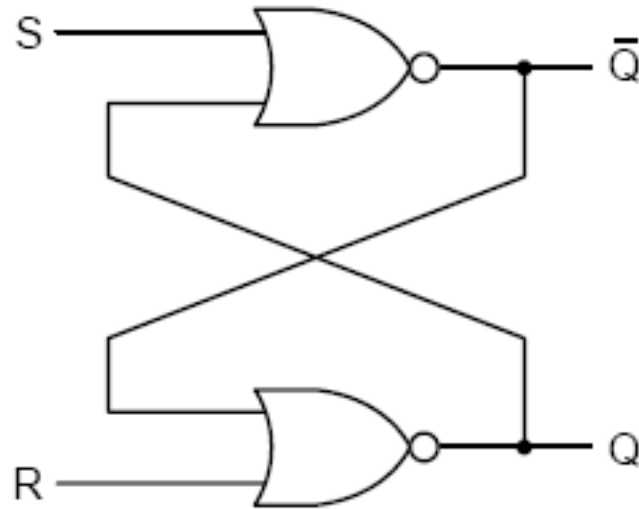
# Combinational logic

- Circuits whose outputs are pure functions of its inputs
- Logical gates (AND, OR, NOT, XOR, etc.)
- Decoders, multiplexers, adders, ALUs

# State Elements

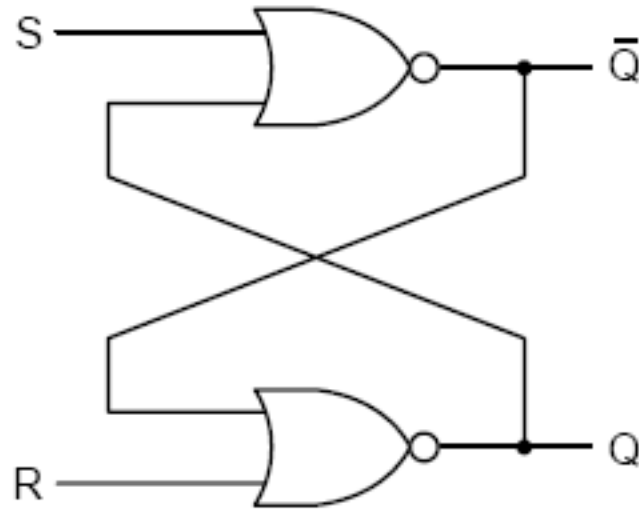
- Output depends on input, AND a value saved inside the element
- State elements have *memory*

# Set-Reset (S-R) Latch



- Output (Q) depends on S, R, AND previous value of Q
- Stores 1 bit of state
- Output Q can change over time: changing inputs S or R can cause Q to change which causes the inputs to the NOR gates to change which can cause Q to change and so on

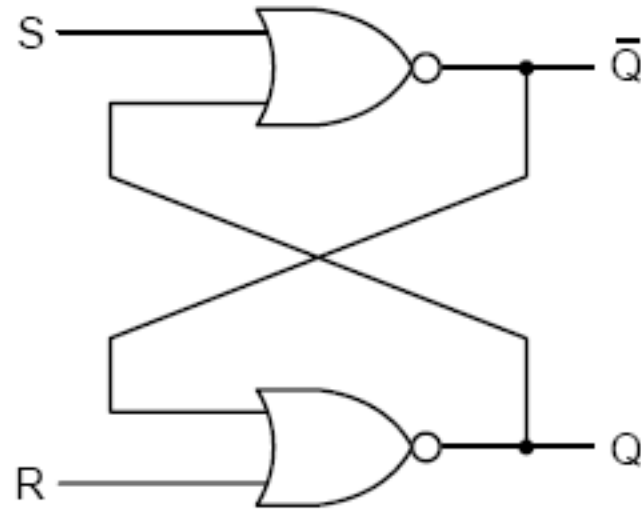
# S-R Latch: $S = 1, R = 0$



Consider what happens when  $Q = 0$  initially and when  $Q = 1$  initially

	Q
A	0
B	1
C	Q from before
D	$\bar{Q}$ from before
E	None of the above

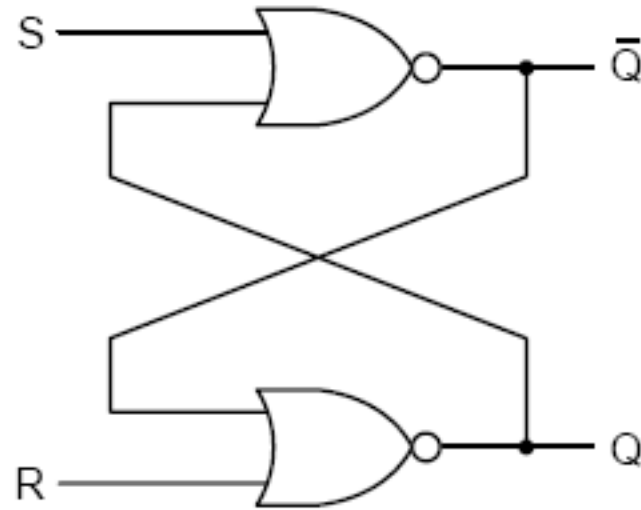
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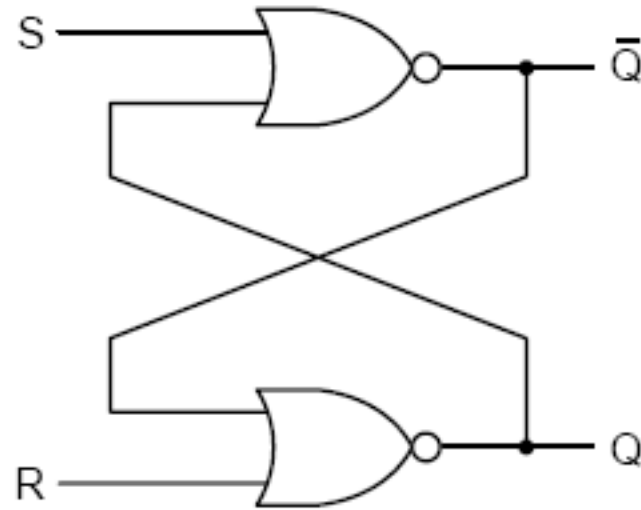
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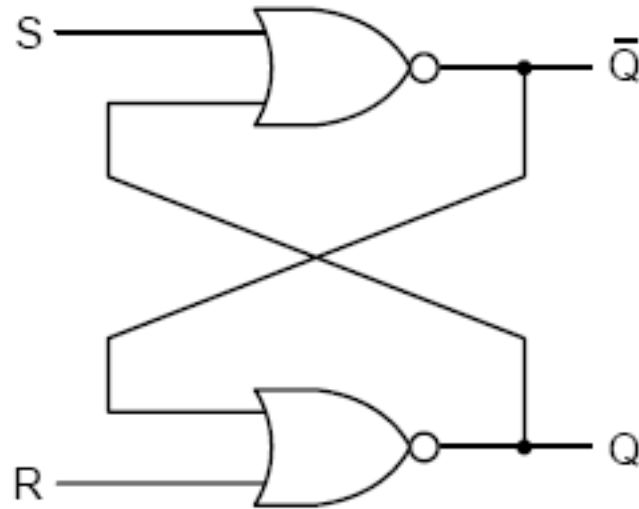
# S-R Latch: $S = 1, R = 1$



	Q	$\bar{Q}$
A	0	1
B	1	0
C	Q from before	$\bar{Q}$ from before
D	$\bar{Q}$ from before	Q from before
E	None of the above	



# S-R Latch



- Set:  $Q_t = 1$
- Reset:  $Q_t = 0$
- Otherwise,  $Q_t = Q_{t-1}$

# Terminology

- The S-R latch is a **bistable multivibrator**
  - **Bistable**: two stable states—set  $Q = 1, \bar{Q} = 0$  and reset  $Q = 0, \bar{Q} = 1$
  - Monostable: one stable state, one unstable state; the circuit returns to the stable state after a short time in the unstable state
  - Astable: two unstable states and the circuit switches between them
  - **Multivibrator**: a digital circuit that uses feedback
    - The name comes from the first such circuit that produced a square wave which had many harmonics, hence *multivibrateur*

# Clock



- Oscillates between 1 and 0 at a set rate
- Used with elements that have memory

# Clocked SR Latch

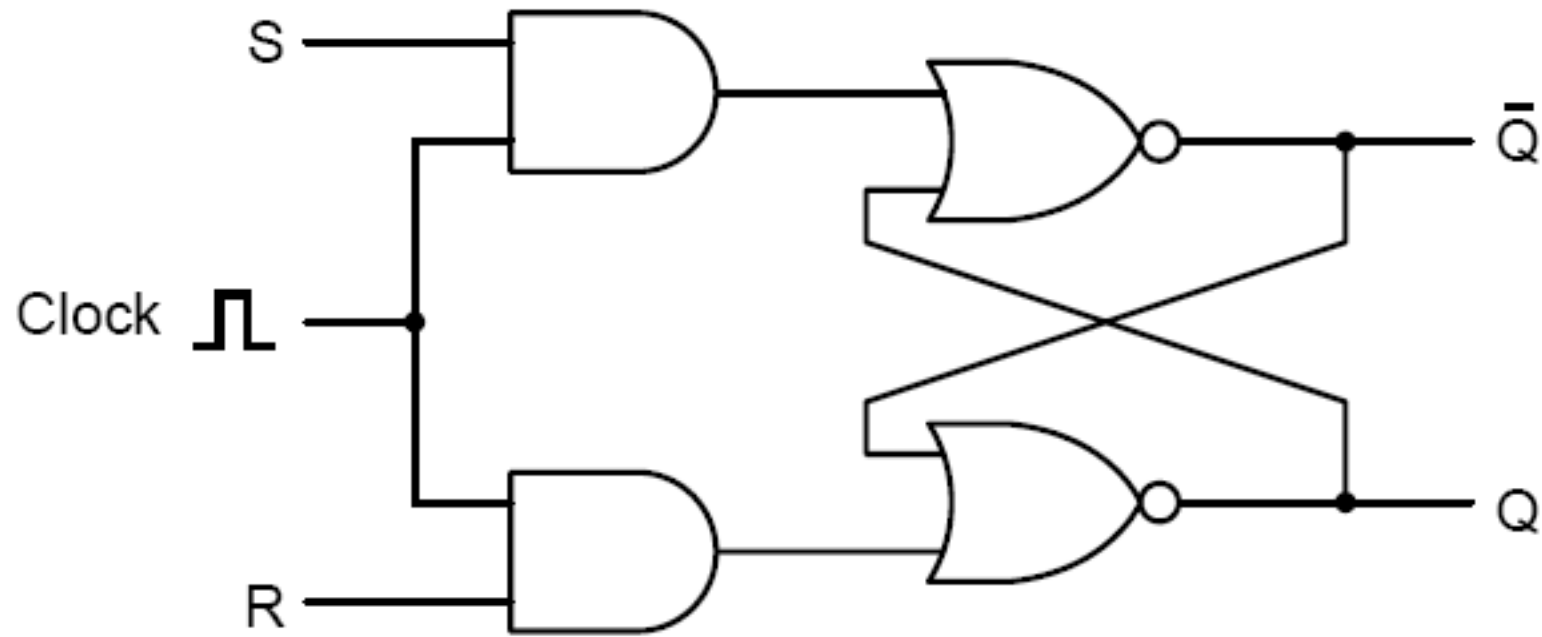


Figure 3-23. A clocked SR latch.

- Only changes state when the clock is asserted

Given S, R and Clock, Q will be:

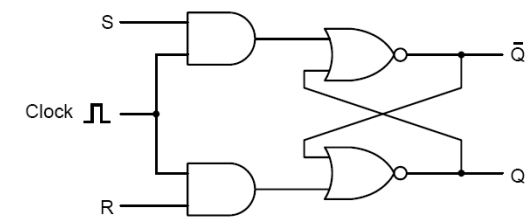
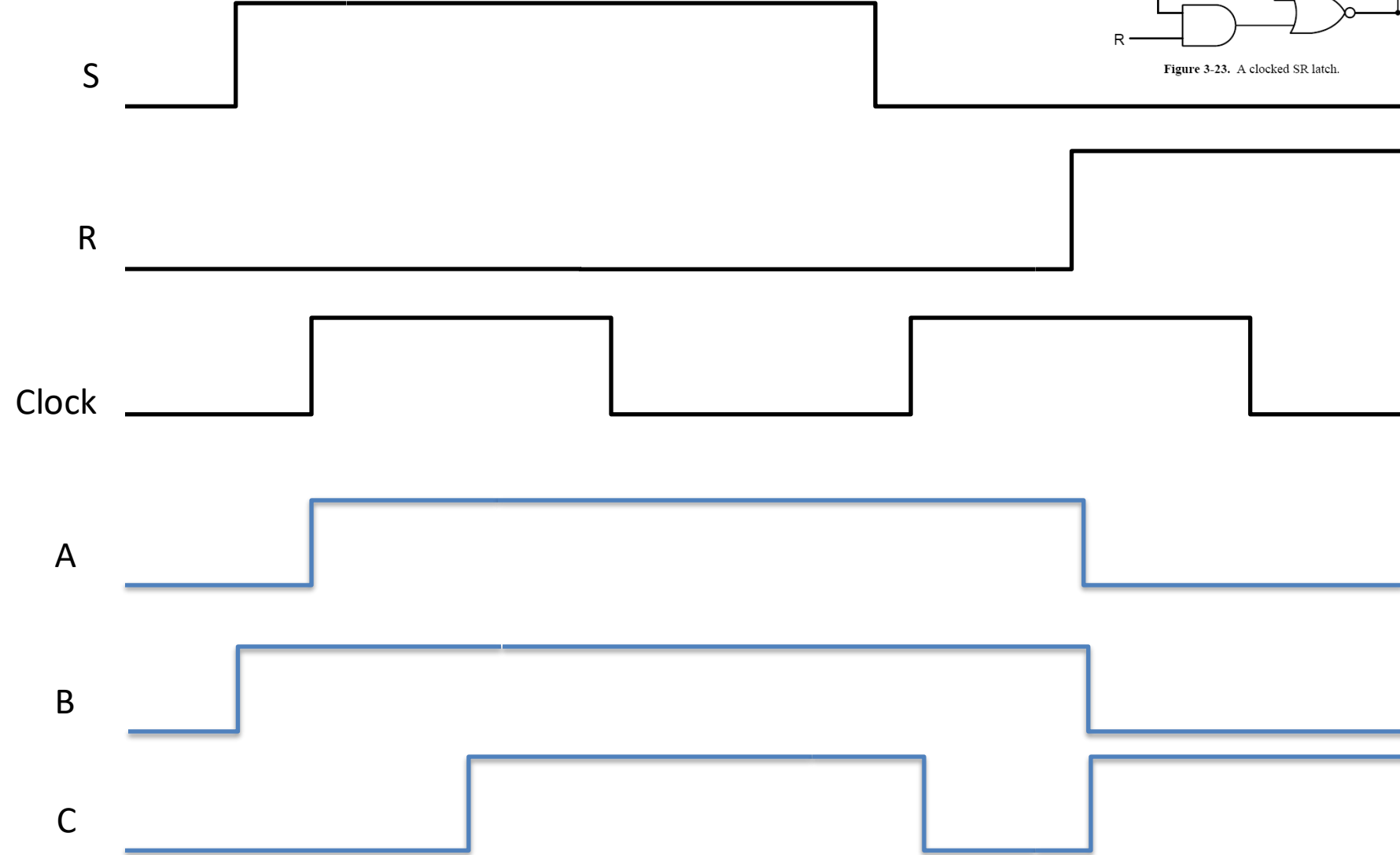


Figure 3-23. A clocked SR latch.



D. None of the above